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RELIABLE DATA AWARE SRAM CELL USING FinFET TECHNOLOGY

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ABSTRACT

The low power and high performance Static Random Access Memory (SRAM) is the main constraint in modern VLSI systems. The SRAM cell power dissipation can be controlled to improve the system power, performance and reliability at a significant level. This research proposes a new technique of Reliable Data Aware (RDA) SRAM cell design using 14 nm FinFET technology to minimize the power dissipation, access delay for read and write operations and maximize the read stability. The proposed FinFET based SRAM design has been employed in RDA SRAM cell and the results analysis proved that the write power dissipation has reduced to 90.14% and read power is about 49.94% than the 6T cell. The read access time and stability of the suggested RDA cell have been improved.

Keyword: FinFET, SRAM cell, power, performance, leakage current, stability.

1. INTRODUCTION

In the last decade, the development of System-on-Chip (SoC) memories has been radically increasing. The Wireless Sensor Networks (WSN) applications in healthcare, military, agriculture and manufacturing industries have been consistently demanding the extended operational lifetime of the battery device. Similarly, today's Internet-of-Things (IoT) applications and portable gadgets demand faster, stable and an increased memory capacity to store the data and further on processing. The IoT applications, WSN applications, use of portable gadgets such as smart phones, PDAs and mobile appliances have become as the common aspect of our daily life. Especially, the use of mobile devices has become so common in everyone's life. Presently, there are many mobile gadgets released every day with fascinating and very attractive specification and features with rapid improvements. Every new release of these new devices highly demands the sustainability as well as the unique success of the respective device [1]. All these devices are designed to process large volume of media data and especially on live streaming. The use and demand for fixed memory access is continuously increasing with higher demand to process video, audio and image implementations can affect the power consumption and the limitation of its battery lifetime.

There are so many SRAM cells with high speed and low power characteristics are being consistently designed and evaluated to meet the continuous and constant industry requirements with respect to the latest developments of VLSI circuits [1, 2]. SRAM cells always play an important role to improve VLSI's performances [3-7]. Though the supply voltage and power consumption are decreased proportionally, the respective speed and static noise margin (SNM) are degraded. There were many SRAM cells proposed earlier [7-10] to improve the SNM. Lately, FinFET has become a mainstream IC technology due to its significant performance improvement and leakage reduction compared to the flat-panel CMOS technology [11].

In this research, a new RDA SRAM cell has been proposed which is designed in FinFET technology. To enhance performance and stability, the proposed SRAM is designed with two circuits for write and read operations. During the write operation, the latch circuit is disconnected to switch the data quicker on the nodes and the lower discharging activity at the bit lines causes low power consumption. This paper is organized as follows. The Section 2 explains the architecture of the proposed cell. The analysis of simulation results and comparisons are highlighted in Section 3. The conclusion is highlighted in Section 4.

2. PROPOSED RDA SRAM DESIGN

The proposed RDA cell aims to decrease the power consumption without any tradeoff between the stability and read access time. There are eight-transistors (8T) through FinFETs are used to design the proposed RDA cell in 14nm submicron technology including a separate circuit for read operation as shown in Figure-1. The proposed cell contains two inverters; namely inverter invL and invR. The two transistors P1 and N1 through FinFETs form the invL, and inverter invR uses another two transistors P2 and N2 through FinFETs.

The nodes QB and Q with corresponding bit-lines BL and BLB are connected by using the N3 and N4 transistors through FinFETs as the access transistors. The write mode operation is performed by WL1, WL2, WS and W signals in the RDA cell. While the write mode operation, the N5 transistor's control signal W is set to low which breaks the feedback connection of the cell so that respective data can be transferred on the nodes QB and Q faster. The read operation is performed by a separate read circuit which consists of transistor N6 through FinFET to improve the proposed cell's read stability. The Read Word Line (RWL) is controlled by the read pass-transistor N6 through FinFET. The signal W is set to high to store the latch property of the cell during the hold and read mode operations. The Static Noise Margin (SNM) of the RDA cell is improved through the segregation of nodes from bit-lines while hold/read mode.

Write mode

The dynamic nature of the cell does the switching of the data at the nodes easily by transistor N5. The Word lines either WL1 or WL2 is asserted to high once the data is set on the bit-lines BL and BLB. The WS signal plays a major role to enhance the write ability instead of WL1 and WL2. In write '1' mode, the bit-line BL and WS are set to high and then assert WL1=V_{DD} to write "1". The transistor N2 is turned on and P2 is turned off. Therefore, voltage at node QB =0 without allowing BLB to discharge.

In order to write "0", the bit-line BLB is set to high, set WS=0 and then assert WL2=V_{DD}. So that the transistor N2 is turned off, hence voltage at node QB=1 without allowing BL to discharge. Due to the influence of WL1, WL2 and WS signal, the discharging activities of bit-lines (BL and BLB) are minimized. Therefore, the active power consumption and write delay are reasonably reduced.

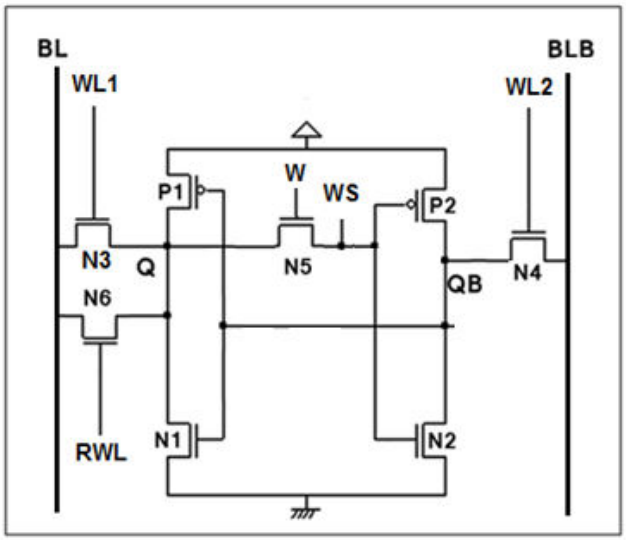


Figure-1. RDA SRAM cell.

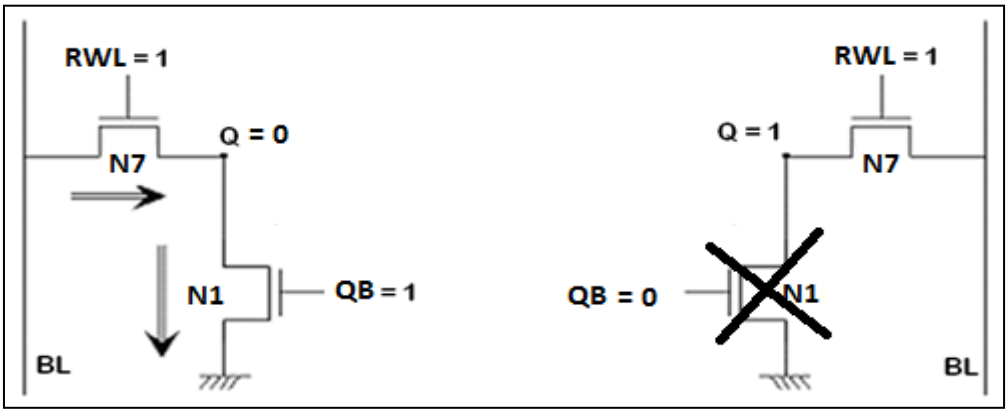


Figure-2. Read '0' and Read '1' operations.

Read mode

For the read operation, the word lines WL1 and WL2 are set to 0 and W is set to 1. The read circuit is comprised of the transistors N6 and N1 as shown in Figure-2. The read operation is performed when the transistor N1 is controlled by node QB and then asserting RWL to high. For read '1' operation, N1 is off (QB=0), switch the node Q to high which results minimum power dissipation. For read '0'mode, the transistor N1 turns on (QB=1). Therefore, BL is discharging through tansistors N6 and N1.

3. RESULT AND DISCUSSIONS

The simulation results of RDA FinFET based SRAM cell's are analyzed in terms of write/read power, write/read delay and stability using FinFET based 14nm submicron technology and presented in this section. The conventional 6T cell consumes more power due to discharge activity of two bit-lines. On the other hand in 7T SRAM cell, the write '0'power consumption is less due to one bit line [4]. Whereas, in the RDA cell either BL or BLB is isolated by WL1 and WL2 from the node Q/QB. This leads to no discharging activity at the bit-lines which causes the write power, write delay as well as leakage current minimize as shown in the Table 1(a), 1(b) and 1(c).

Table-1. (a) Write power (b) Access time and (c) Leakage current.

(a)

Write power consumption (µw)			
Transitions	**6T**	**7T**	**RDA**
Write '1'	5.202	5.202	0.485
Write '0'	5.192	0.539	0.539

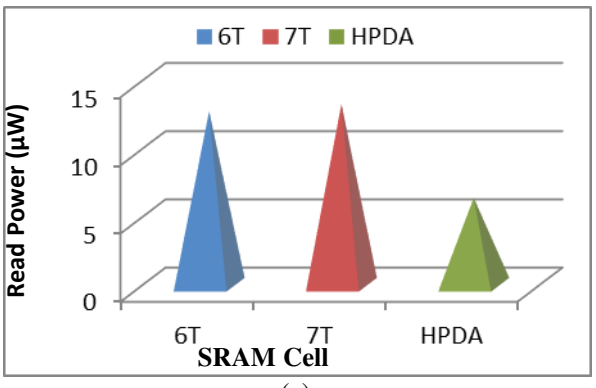
(b)

SRAM cell	**Read delay** (*ps*)		**Write delay** (*ps*)	
	Read '0'	**Read '1'**	**Write '0'**	**Write '1'**
6T	84.6	85.4	54.2	54.2
7T	85.3	85.6	55.0	30.0
RDA	45.4	-	40.0	30.0

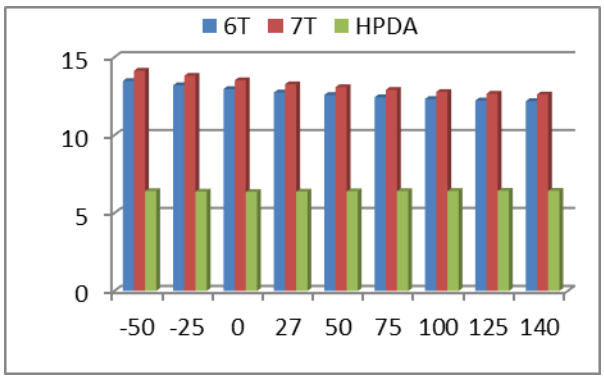
(c)

SRAM cell/transistor		Write operation	
	Current	Write '0'	Write '1'
6T	I_{N2}	0.015mA	0.015mA
	I_{N3}	0.015mA	0.015mA
	I_{N4}	0.015mA	0.05mA
	I_{N5}	0.05mA	0.015mA
	I_{P1}	0.048mA	0.049mA
	I_{P2}	0.049mA	0.05mA
RDA	I_{N1}	0.106nA	0.106nA
	I_{N2}	0.202mA	0.405nA
	I_{N3}	0.405nA	0.229mA
	I_{N4}	0.106nA	0.111nA
	I_{N5}	0.106nA	0.111nA
	I_{N6}	0.106nA	0.106nA
	I_{P1}	0.175mA	0.201nA
	I_{P2}	0.201nA	0.178mA

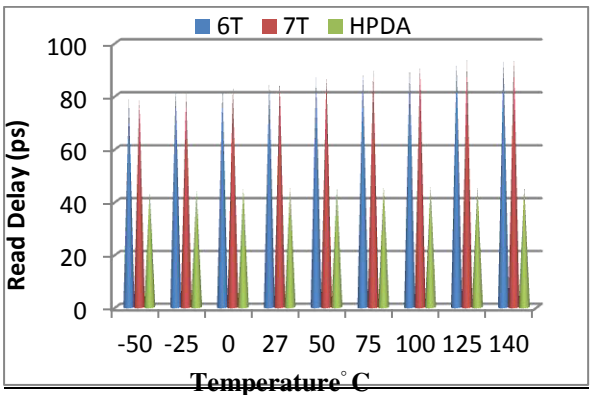
In read '0' mode, N6 and N1 are turned on and BL is discharging. So that the average read power dissipation is same as 6T cell. During the read '1' mode, the transistor N1 is turned off and there is no discharging read path which influences about 50% average power/delay reduction as illustrated in Figure-3(a). As temperature varies from -50˚C to 140˚C, the read power and read delay of the RDA cell variations are minimum as shown in Figure-3(b) and 3(c). The Figure-3(d) shows that the read stability of the proposed cell is 2.86x improved than the conventional cell because of the separate read circuit.



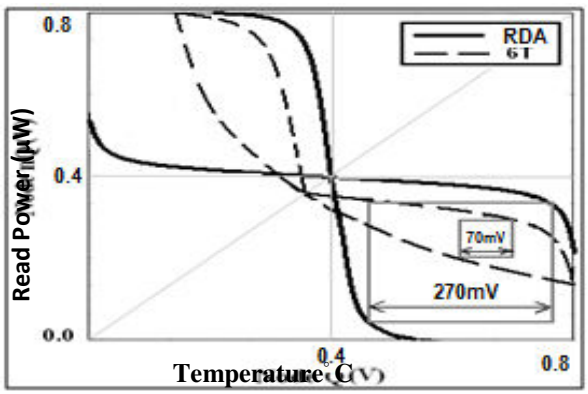
(a)



(b)



(c)



(d)

Figure-3. (a) Read power (b) Read power with different temperature (c) Read delay with different temperature and (d) Static Noise Margin.

4. CONCLUSIONS

The proposed FinFET based RDA SRAM cell results have confirmed to improve the read and write performance. The read and write power are saved compared to 6T cell about 49.94% and 90.14% respectively. The separate circuit for read and write operations influence the read stability improvement as well as lesser read power consumption due to low leakage current. Even in worse condition with temperature ranging from -50˚C to 140˚C, the power loss of the proposed cell is proved to be minimum during the read mode.

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