VOL. 14, NO. 1, JANUARY 2019 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

SPEED CONTROL ANALYSIS OF LSCPWM DRIVEN SEVEN-LEVEL INVERTER FED PERMANENT MAGNET SYNCHRONOUS MOTOR DRIVE

R. Sasidhar and A. Lakshmi Devi
Department of Electrical and Electronics Engineering, Sri Venkateswara University College of Engineering, Tirupati, AP, India
E-Mail: sasidhar1.eee@gmail.com

ABSTRACT

Realization of inverter fed electric motors is made possible with the trends in power electronic technology. Permanent magnet synchronous motor (PMSM) is one motor replaced conventional electric motors with attractive features like compactness, lightweight and efficiency. The paper presents the analysis of seven-level diode clamped multi-level inverter fed PMSM. Seven-level diode clamped inverter is driven from pulse generator employing level-shifted (multi) carrier PWM pattern. Reference current signal is generated from closed-loop control of PMSM. Closed-loop speed control is presented in detail. The presented concept is analyzed with PMSM running with fixed speed and variable speed conditions. LSCPWM Driven Seven-Level Inverter Fed Permanent Magnet Synchronous Motor is developed and result analysis is presented using MATLAB/SIMULINK software.

Keywords: PMSM, seven-level, LSCPWM, closed-loop, control, speed.

INTRODUCTION

With the latest growth in power electronic technology, conception of motor drives [1-3] is achieved replacing conventional motors. Motor drive technology is revolutionary making human efforts easier. Brushless DC (BLDC) motors and permanent magnet synchronous motor (PMSM) are among them. The mentioned motors, having sophisticated design trends the motor drive applications in many industries and commercial purpose. PMSM motor consists of a permanent magnet, which rotates (the rotor), surrounded by equally spaced windings, which are fixed (the stator). Current flow in each winding (when excited) produces a magnetic field vector, which sums with the fields from the other windings. By controlling currents in the stator windings, a magnetic field of arbitrary direction and magnitude is produced by the stator. Torque is then produced by the attraction or repulsion between this net stator field and the magnetic field of the rotor. Principle of operation is similar to that of synchronous motor but the rotor consists of permanent magnets in PMSM [4-6].

Stator windings of PMSM are distributed winding and the back EMF (BEMF) is sinusoidal in shape [7-10]. Permanent magnet rotors provide sinusoidal flux distribution in the air gap, making the BEMF a sinusoidal shape. Depending on how magnets are attached to the rotor, PMSM motors can be classified into two types: surface PMSM (SPMSM) and interior PMSM (IPMSM). SPMSM mounts all magnet pieces on the surface, and IPMSM places magnets inside the rotor.

PMSM motors are generally fed from sinusoidal source. If PMSM is to be fed from a DC source, inverter (DC-AC) does the job of supplying sinusoidal excitation to phase windings of PMSM. Conventional inverters (two-level or square wave) suffer from high dv/dt across switch resulting in high switching losses. High switching losses reduces the efficiency of the converter.

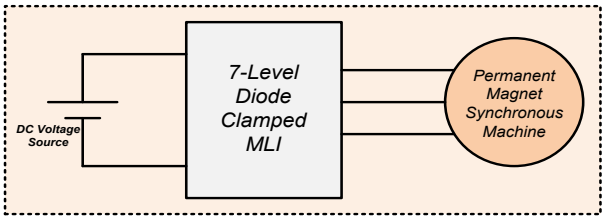

Figure-1. Representation of 7-level inverter fed PMSM.

Conventional inverters give out square wave alternating output voltage consisting of high distortion. Alternating quantity with high distortion cannot be fed to any device and needs smoothing filters. Inverters are made up of capacitors and inductors which make the output current smooth as compared to switching square wave output we get with a conventional inverter. If the distortion quantity is high, filter size also increases. This phenomenon led to development of multi-level inverters.

Now-a-days multi-level inverters became the prior pick in many of the industries for high power high voltage applications. Multi-level inverters are able to generate high voltage with lower rated devices. Multi-level inverter generates leveled (stepped) output and as the number of level increases better output voltage waveform is obtained. Diode clamped multi-level inverters are one among multi-level topologies and uses diodes as clamping elements. Multi-level inverter driven PMSM is shown in Figure-1.

The paper presents the analysis of seven-level diode clamped multi-level inverter fed PMSM. Seven-level diode clamped inverter is driven from pulse generator employing level-shifted (multi) carrier PWM pattern. Reference current signal is generated from closed-loop control of PMSM. Closed-loop speed control is presented in detail. The presented concept is analyzed with PMSM running with fixed speed and variable speed conditions.

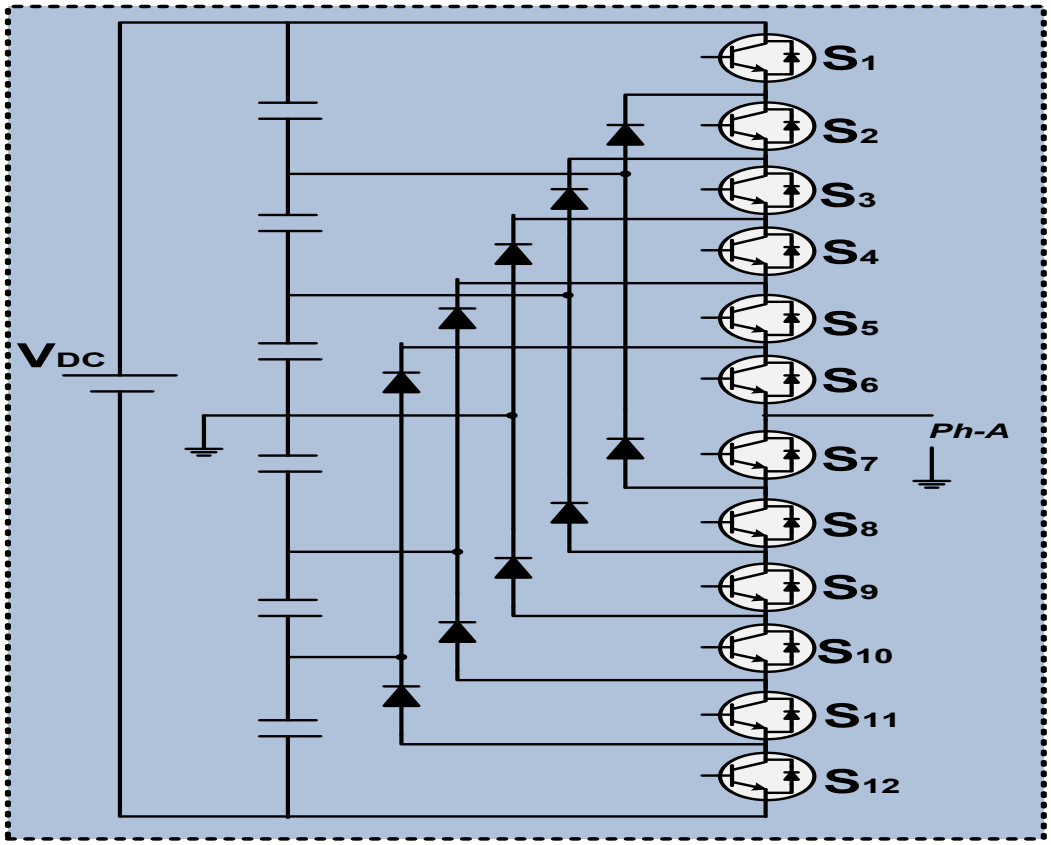

Figure-2. 7-level diode clamped inverter.

Table-1. Switching table in 7-level DCMLI.

Voltage Level	Switching state											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

SEVEN-LEVEL DIODE CLAMPED INVERTER FED PMSM

Diode clamped inverter (DCMLI) is one among topologies of basic multi-level inverters. DCMLI uses diodes and gives different voltage levels to the capacitor banks connected in series. The benefit of using diode is to reduce stress on other electrical devices because it gives a limited amount of voltage. The main drawback of this topology is the maximum voltage which can be obtained from DCMLI cannot be more than half of input voltage (DC voltage). This drawback can be solved by increasing the number of capacitors, switches and diodes. This type of inverters provides the high efficiency and it is a simple method of the back to back power transfer systems.

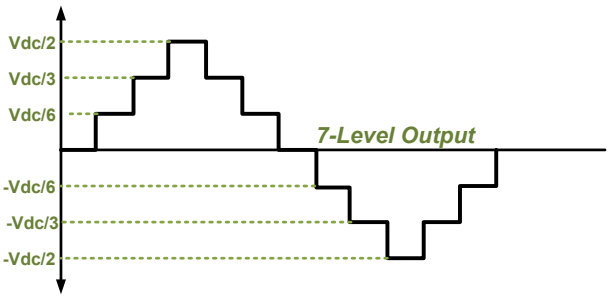

Figure-3. Seven-level output of DCMLI.

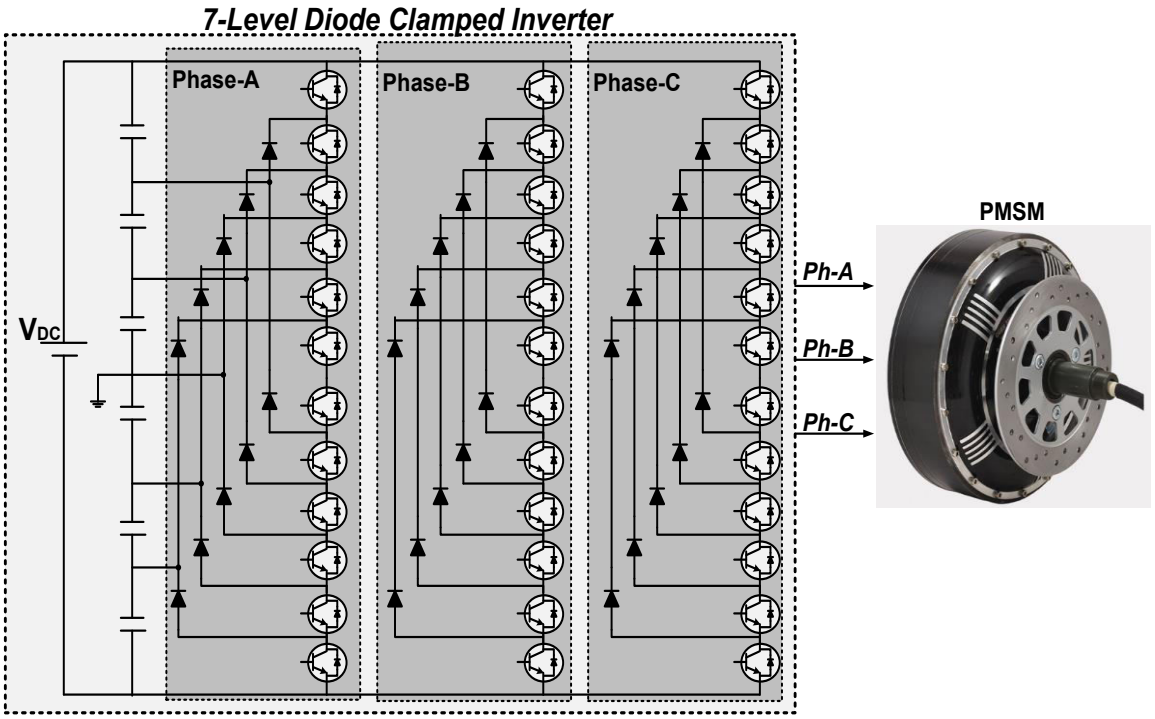

Figure-4. Seven-level DCMLI fed PMSM.

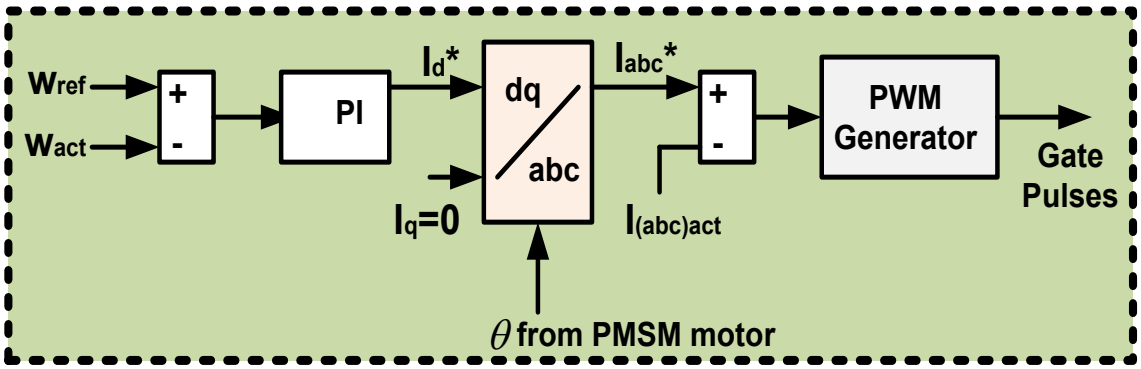

Figure-5. Control strategy for PMSM drive.

Seven-level DCMLI is shown in Figure-2. For the convenience, only one phase of DCMLI is represented in Figure-2 and similar two phases connected in similar fashion forms a three-phase DCMLI. Seven-level DCMLI consists of twelve power switches, ten diodes and six capacitors. Power switches are generally IGBT's. The main DC voltage source is split equally across all the six capacitors to give leveled output waveform. Table I illustrates the switching states of twelve power switches in seven-level DCMLI to give out 7-level stepped output waveform. Sequential switching of power switches in phase yields 7-level output as shown in Figure-3.

CONTROL OF PMSM DRIVE

The control strategy involves simple arithmetic calculations and blocks to control the speed of PMSM. Control algorithm accepts mechanical feedback from the PMSM to generate reference currents for the pulse generation.

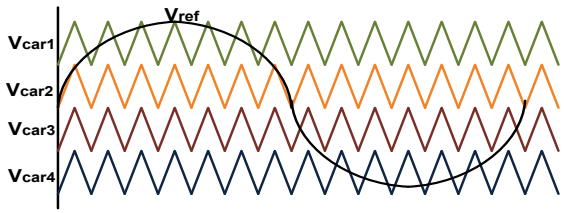

Figure-6. LSCPWM pattern.

Actual speed of the PMSM is sensed and is compared to the reference speed signal. The error in speed is fed to PI controller. PI controller reduces the error signal and generates direct axis component of current signal. Quadrature component of current is considered to be zero. Both the quadrature and direct axes components are processed to inverse Park's transformation to generate reference current signal in 'abc' co-ordinate system.

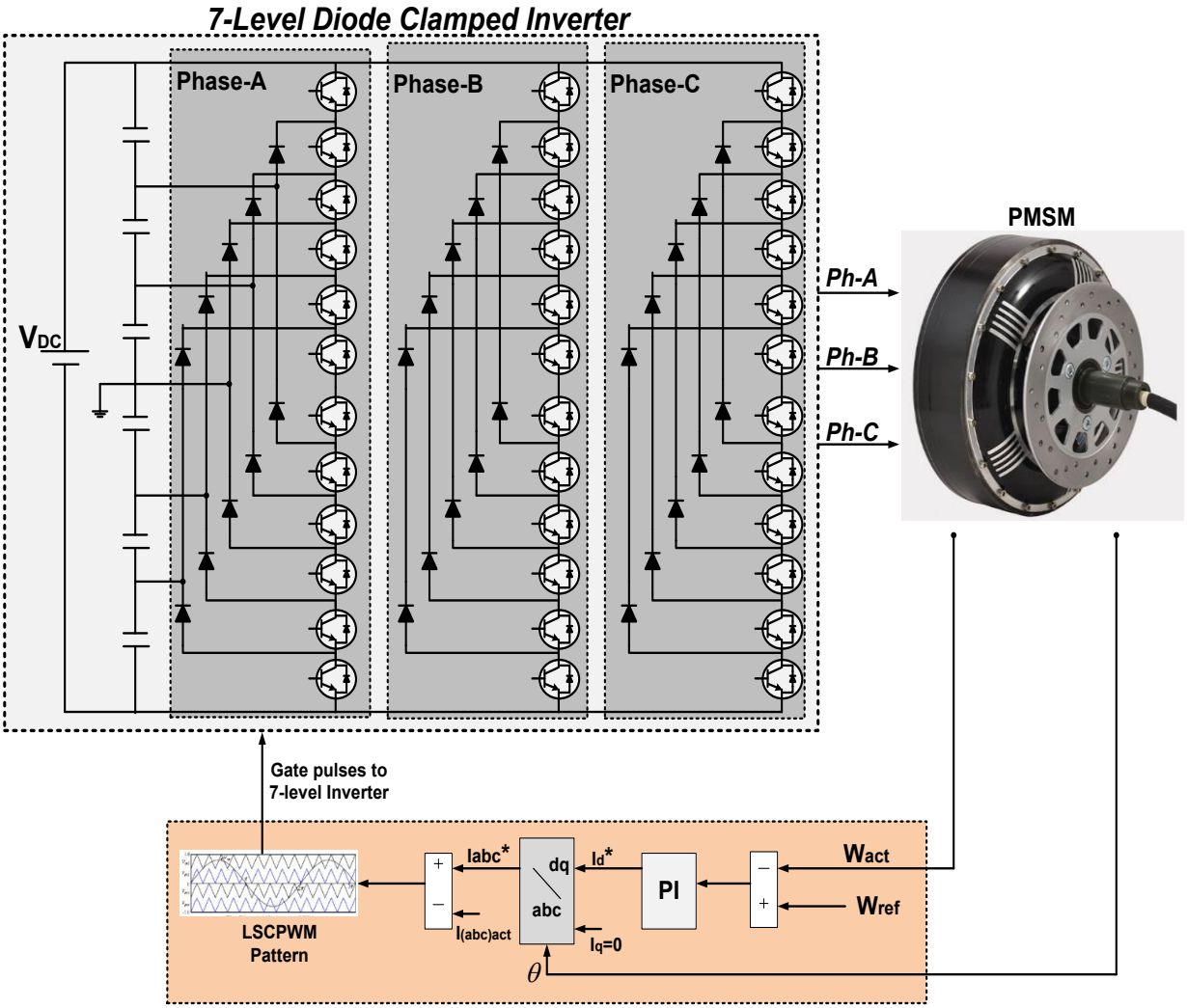

Figure-7. Schematic arrangement of seven-level DCMLI fed PMSM with speed control.

Angular position of rotor from PMSM is fed to inverse Park's transformation through position sensor. The generated reference currents are now compared to actual currents and the error signal is sent to PWM generator. Multi-carrier (level shifted) PWM pattern is employed to generate gate pulses to power switches of 7-level DCMLI. The complete control algorithm to control PMSM is shown in Figure-5 and Figure-6 illustrates the LSCPWM pattern to trigger power switches of DCMLI. LSCPWM pattern consists of high-frequency carrier signals. Reference signal when overlapped with carrier waveforms generates triggering pulse at the point of intersection. The complete schematic arrangement of seven-level DCMLI fed PMSM with speed control is illustrated in Figure-7. Table-2 represents system parameters.

RESULT ANALYSIS

Table-2. System parameters of DCMLI fed PMSM with closed-loop speed control system.

Parameter	Value
Inverter DC source voltage	500 V
PMSM stator phase resistance	18.7 Ohms
Load Torque	5 N-m
Reference signal frequency	50 Hz
Carrier signal frequency	15.05 KHz

Case 1: PMSM with fixed speed

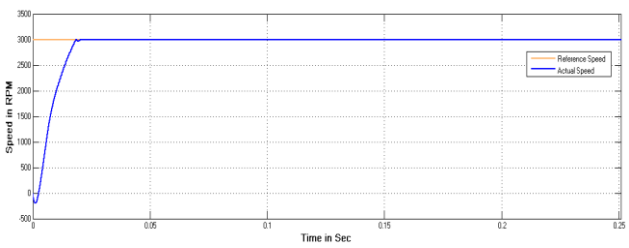

Figure-8. Speed of PMSM.

Figure-8 illustrates the speed curve of PMSM running with fixed speed condition. Reference speed and actual speed are shown in figure. Actual speed follows the reference speed. PMSM is set to run at constant 3000 RPM and actual speed follows the reference speed.

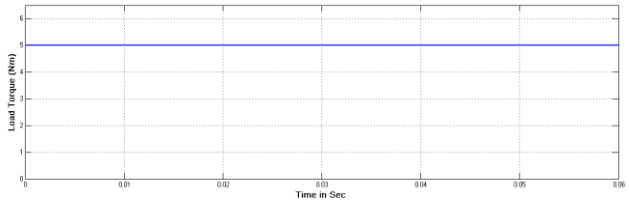

Figure-9. Load torque of PMSM.

Figure-9 illustrates the load torque impressed on PMSM. Load torque of 5 Nm is impressed on PMSM.

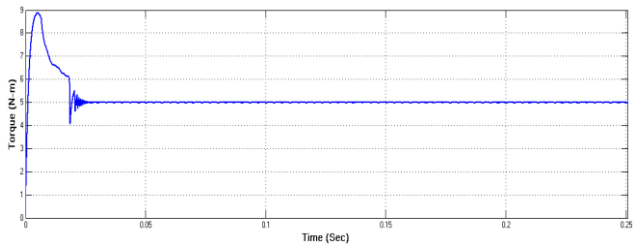

Figure-10. Torque generated by PMSM.

Figure-10 shows the torque curve generated by PMSM. Torque of 5 Nm is generated to meet the load torque as shown in figure.

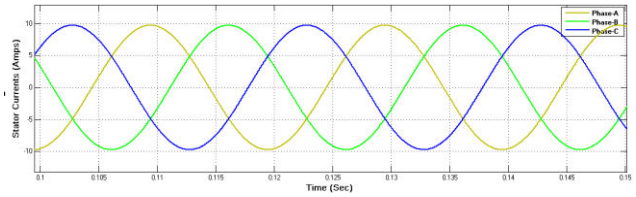

Figure-11. Stator currents of PMSM.

Figure-11 shows three-phase stator currents of PMSM. Three-phase stator currents are balanced sinusoidal with 10A peak.

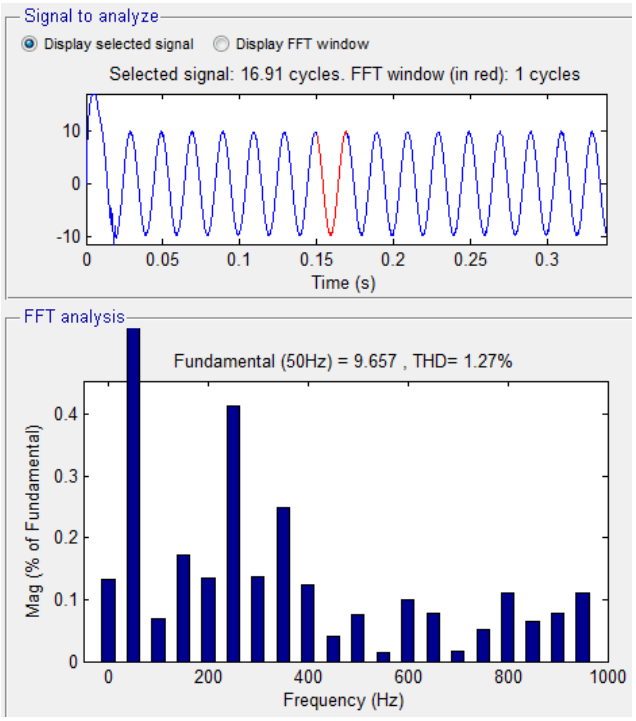

Figure-12. THD in stator currents.

Figure-12 shows the FFT window of harmonic distortion in stator currents. Stator currents are distorted by 1.27% with respect to fundamental and distortion is very less illustrating sinusoidal excitation to PMSM.

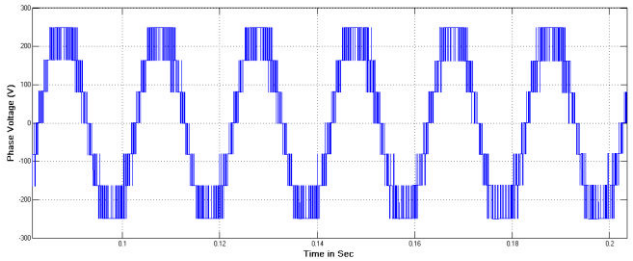

Figure-13. Output phase voltage of DCMLI.

Figure-13 shows the output phase voltage of diode clamped inverter. Diode clamped inverter generates only half the amount of DC voltage source. DC voltage fed to DCMLI is 500V and phase voltage obtained (in Figure-13) is with peak 250V.

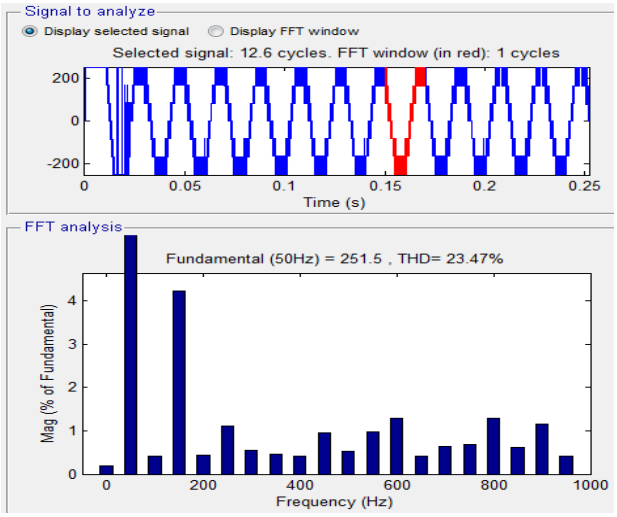

Figure-14. THD in phase voltage of DCMLI.

Figure-14 shows the FFT window for harmonic distortion in phase voltage of DCMLI. Phase voltage of DCMLI is distorted by 23.47%.

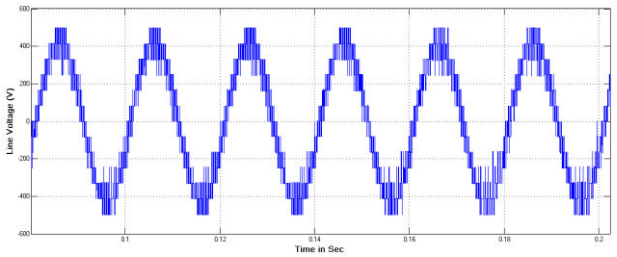

Figure-15. Line voltage of DCMLI.

Figure-15 shows the line voltage of DCMLI. Line voltage peak value is 500V for DCMLI.

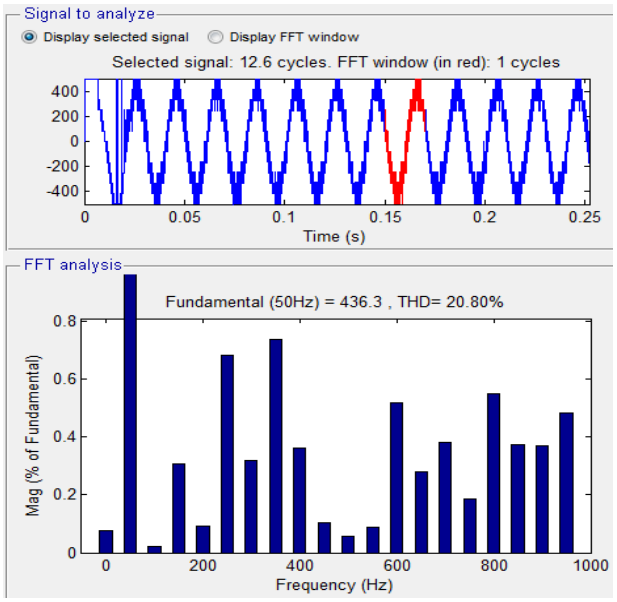

Figure-16. THD of line voltage.

THD FFT window of line voltage is shown in Figure-16. Line voltage is distorted by 20.80%.

Case 2: PMSM with variable speed

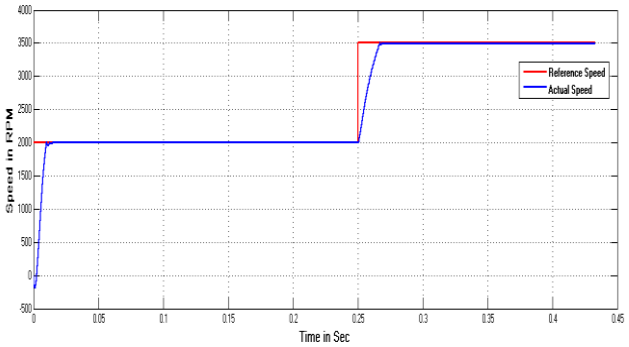

Figure-17. Speed of PMSM.

Figure-17 illustrates the speed curve of PMSM running with variable speed condition. Reference speed and actual speed are shown in figure. Actual speed follows the reference speed. PMSM is set to run at constant 2000 RPM initially and actual speed follows the reference speed. After prescribed time 0.25 sec, set speed changes to 3500RPM and actual speed follows reference value.

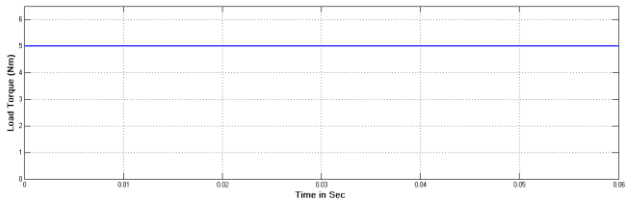

Figure-18. Load torque of PMSM.

Figure-18 illustrates the load torque impressed on PMSM. Load torque of 5 Nm is impressed on PMSM.

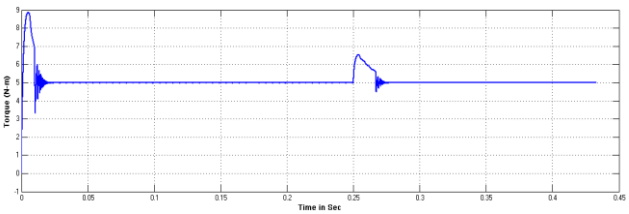

Figure-19. Torque generated by PMSM.

Figure-19 shows the torque curve generated by PMSM. Torque of 5 Nm is generated to meet the load torque as shown in figure. At speed variation time 0.25 sec, there is a slight distortion in torque else constant.

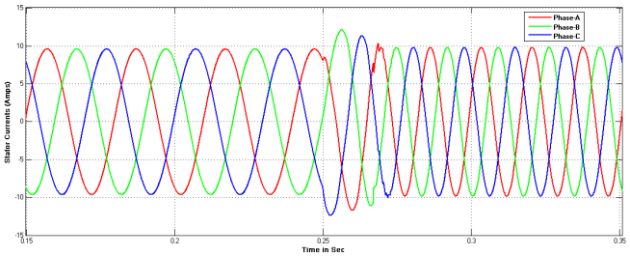

Figure-20. Stator currents of PMSM.

Figure-20 shows three-phase stator currents of PMSM. Three-phase stator currents are balanced sinusoidal with 10A peak. Since speed is proportional to frequency, after speed variation time 0.25sec, the frequency of stator current increases as shown in figure.

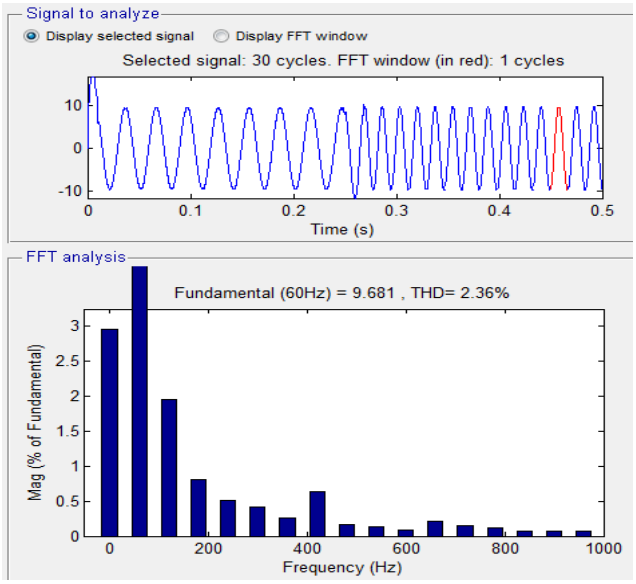

Figure-21. THD in stator currents.

Figure-21 shows the FFT window of harmonic distortion in stator currents. Stator currents are distorted by 2.36% with respect to fundamental and distortion is very less illustrating sinusoidal excitation to PMSM.

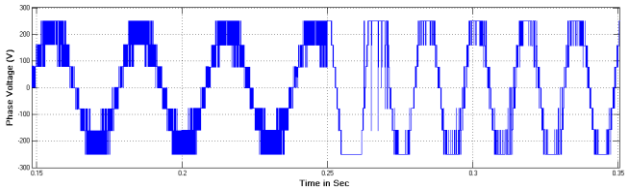

Figure-22. Output phase voltage of DCMLI.

Figure-22 shows the output phase voltage of diode clamped inverter. Diode clamped inverter generates only half the amount of DC voltage source. DC voltage fed to DCMLI is 500V and phase voltage obtained (in Figure-13) is with peak 250V. Since speed is proportional to frequency, after speed variation time 0.25sec, the frequency of phase voltage increases as shown in figure.

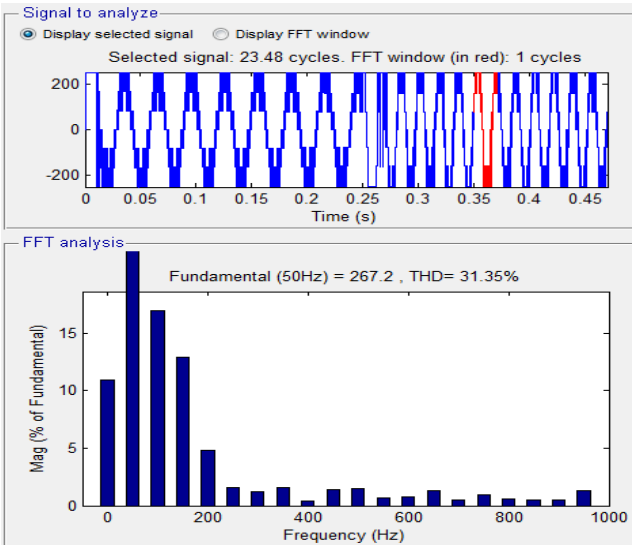

Figure-23. THD in phase voltage of DCMLI.

Figure-23 shows the FFT window for harmonic distortion in phase voltage of DCMLI. Phase voltage of DCMLI is distorted by 31.35%.

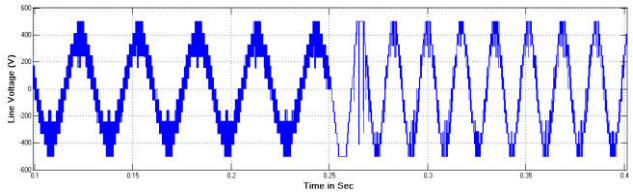

Figure-24. Line voltage of DCMLI.

Figure-24 shows the line voltage of DCMLI. Line voltage peak value is 500V for DCMLI. Since speed is proportional to frequency, after speed variation time 0.25sec, the frequency of line voltage increases as shown in Figure.

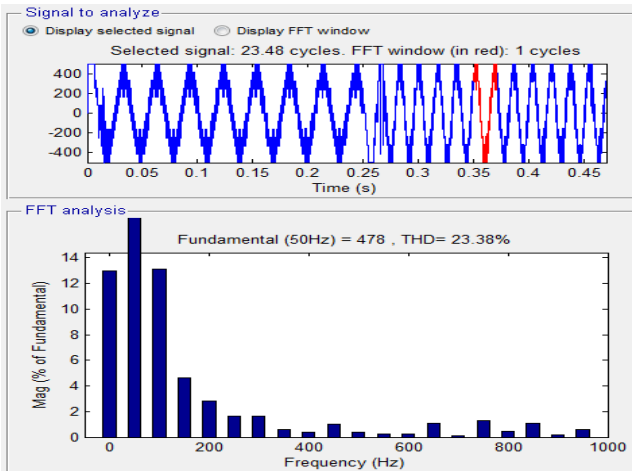

Figure-25. THD of line voltage.

THD FFT window of line voltage is shown in Figure-25. Line voltage is distorted by 23.38%.

Table-3 shows the comparison of harmonic distortion analysis with different running conditions of PMSM.

Table-3. Comparison of THD.

THD	Fixed speed mode	Variable speed mode
Stator current of PMSM	1.27 %	2.36 %
Phase voltage of inverter	23.47%	31.35%
Line voltage of inverter	20.80%	23.38%

CONCLUSIONS

Power electronic technology has made motor drive control easier. PMSM is one of the machines employed in many applications due to its meritorious advantages over conventional machines. This paper presents PMSM driven with seven-level diode clamped inverter. Characteristics of seven-level DCMLI are shown. PMSM characteristics are shown with fixed and variable speed operating conditions. The control algorithm presented effectively controls the speed of PMSM in fixed and variable speed conditions. In-phase LSCPWM multi-carrier PWM drives power switches of DCMLI. THD analysis is compared for different running conditions of PMSM. Stator current is distorted by very less quantity implies sinusoidal excitation is supplied to phase windings of PMSM.

REFERENCES

[1] Paul C. Krause, Oleg Wasynczuk and Scott D. Sundhoff. Analysis of Electric Machinery and Drive Systems. IEEE Press Power Engineering society ISBN-0-471-14326-X.

[2] R. Krishnan. Permanent Magnet Synchronous and Brushless DC Motor Drives. CRC Press, Taylor and Francis Group. ISBN-978-0-8247-53849

[3] H, Madadi Kojabad and G. Ahrabian. 2000. Simulation and analysis of the interior permanent magnet synchronous motor as a brushless AC-drive. Science direct / Simulation practice and theory. 7: 691-707.

[4] R. Dhaouadi, N. Mohan and L. Norum. 1991. Design and implementation of an extended Kalman filter for the state estimation of a permanent magnet -50 1 synchronous motor. IEEE Trans. Industrial Electronics. 6(3 0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1): 491 497.

[5] Pragasan Pillay, R. Krishnan. 1988. Modeling of Permanent Magnet Motor Drives. IEEE. 35(4).

[6] K. Rajashekara, A. Kawamura and K. Matsuse. 1996. Sensorless control of AC motor drives. New York: IEEE Press.

[7] L. Samaranayake, Y. K. Chin and U. S. K. Alahakoon. 2003. Distributed control of permanent magnet synchronous motor drive systems. Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on. 1: 710-715.

[8] G. Sree Lakshmi, S. Kamakshaiah and T. R. Das. 2013. Closed loop PI control of PMSM for hybrid electric vehicle using three level diode clamped inverter for optimal efficiency. Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on, Nagercoil. pp. 754-759.

[9] L. Feng Y. Koren and J. Borenstein. 1993. Cross-Coupling Motion Controller for Mobile Robots. IEEE Trans. on Control Systems Technology. Vol. 1.

[10] H. H. Lee and U. H. Jeong. 2000. A Study on Speed Synchronization for Multi Motors using Controller Area Network. IEEE Trans. Ind. Appl. 44(4).