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LOW POWER CUSTOM CIRCUIT BUILDING USING STANDARD CELLS WITH REDUCED LEAKAGE BY APPLYING GATE LENGTH BIASING TECHNIQUE FOR HIGH END COMPUTING APPLICATIONS

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ABSTRACT

In this paper the concept of leakage power reduction using Gate Length Biasing technique is used. All the CMOS instances used are gate length biased. This paper explains the leakage reduction in a digital circuit which makes use of gate length biased NAND gates to achieve lower power dissipation. All the designs and simulations have done using gpdk 90nm technology and verified using Cadence and Liberate tools. The motive of this paper is clearly indicated using a 8 bit Multiplier Accumulator unit (MAC). The MAC unit consists of several individual blocks: 8 bit multiplier, a 17 bit adder and a 17 bit accumulator. These blocks at various places make use of the modified NAND_GLB gate. These gates are placed away from the critical path. This is because any devices speed or swift working depends upon the delay that occurs in the critical path. So it's always better to keep the delay at the critical path very minimum. Thus the increased threshold devices or the modified devices are placed at other non-critical paths so that the leakage due to those cells is reduced. This path identification is done using an heuristic algorithm. This method thus helps in reducing the major issue of sub threshold leakage. This leakage is due to the direct connection from VDD to GND even when the device is not in use. The power variation that was observed in the MAC units with and without the GLB gates are compared and a reduction of 36% is obtained.

Keywords: standard cell, low leakage design, gate length biasing, characterization.

1. INTRODUCTION

The dissipation in a CMOS occurs in two forms (i) Dynamic energy dissipation and (ii) Static energy dissipation. The energy that is lost due to the charging and discharging phase of the load capacitors are called the dynamic energy dissipation and the short energy dissipations are those which are normally ignored as they occur due to direct connection of power supply to ground. This leakage is found to be high enough in today's electronic devices [1]. An average of 18% in 130nm and 54% in 65nm has been so far measured [12]. While using GLB in 90nm technology reverse SCE called RSCE takes place which reduces the leakage power [3]. There are two means by which power reduction is brought about one is either considering the stand alone part which means those sectors that which wouldn't be using the power supply at that particular time and the other is trying to reduce the runtime leakage [8]. Stand alone has been done by using body biasing and multi Vth methods [4]. Here in this work the main focus is on reducing the runtime leakage which will bring about a better leakage power reduction.

Leakage is of three forms: (i) Sub threshold leakage (ii) gate leakage (iii) reverse biased drain substrate and source substrate junction band to band tunnelling leakage. Sub threshold leakage is the major contributor [5] of the dissipation and it can be overcome in short channel devices by using the gate length biasing technique. As the gate length is increased the threshold voltage increases correspondingly which avoids leakage both during active and stand by modes. This technique tends to increase the delay to a certain level but linearly [10] [13]. The power dissipation decreases exponentially.

The delay penalty in the design is overcome by using a technique called the selective gate length biasing [6]. Here the gate length biased standard cells are used only on paths that aren't included in the critical path [7, 9]. The non-critical paths are identified using a heuristic algorithm. This method thus helps in reducing the total power as well as leads a path to overcome the delay issues. The paper is organized as follows: Section II describes the steps by which the GLB technique has been implemented. Section III brief's about the path till the characterization of the standard cell. Section IV validates the proposed design and explains it features or advantages. Section V concludes the research idea behind the paper.

2. GLB AT CELL-LEVEL

2.1 Creating a library

At the cell level biasing is done by making changes to the device variants. The varied cells are placed only in the non-critical paths so that those cells have low leakage while the ones which actively work still have the normal amount of leakage [11]. The total dissipation is in turn reduced by using this method.

In this biasing methodology only 10% increase is considered making it very usual like any other designs. By varying a little of the channel length only the poly to gate thickness reduces and there is no much changes that might occur in the design schematic and layout. This thus makes the window requirement too easy. Thus manufacturing does not involve much time. This technique has an increase in library size but only to a very little extend. The minimum spacing rule of the DRC rule file is not being violated so it is absolutely acceptable. Here 90nm

technology is being used and the gate length is set to 110nm which brings about a low leakage and no much variation from the nominal V_{th}. This brings about low leakage at every small part that they are being used even though it is at a higher cost.

Here in this paper the standard cell considered is a NAND gate which would be referred as NAND_GLB throughout the paper. The length is chosen in such a way that in which every part they are used they must be able to bring about at least a minimal reduction to the whole power being dissipated. In this case a length of 110nm has been found to be the nominal value. After the small variation is brought about the design is further sent for extraction and power & timing characterization process.

2.2 Concept of sizing for leakage optimization

The concept of sizing has two means downsizing and up sizing. Here downsizing is being used. In this methodology the non-critical paths are identified using the heuristic algorithm and are replaced by the biased variants and the rest of the circuit is placed with the nominal ones. Downsizing has no timing violations and thus leakage minimization is exhibited.

3. PROPOSED DESIGN FLOW

3. 1 cell design flow

The standard cell design procedures are explained with the flow diagram in Figure-1. The schematic of the NAND_GLB cell is drawn. The same is checked for design rule check and layout versus schematic from the layout designed from the schematic. It also explains the metal layers used in the new design.

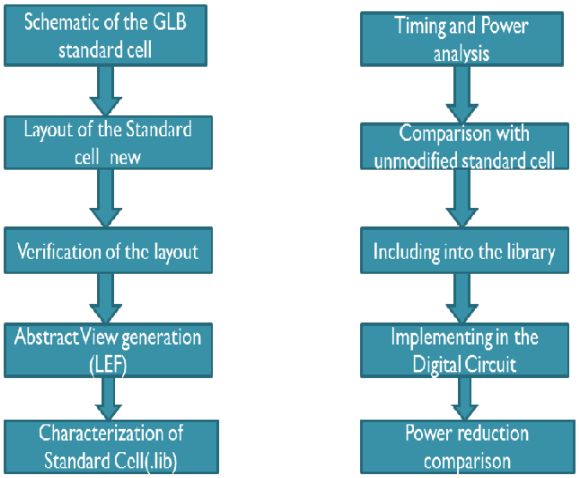

Figure-1. Low leakage standard cell design flow.

3.1.1 Schematic

Using Cadence schematic editor the new standard cell was designed and the length of the channel was changed from 100nm to 110nm. The increase was done with 10nm variation thus to avoid rapid changes. The schematic has the skeleton of the standard cell that is being created. The schematic hold the normal pattern of the NAND gate with 2 PMOS devices in parallel and 2 NMOS in series. The modified and unmodified are drawn for comparison purpose. The schematic for the modified NAND_GLB is shown in the figure below. The simulation roughly indicates the power that a NAND_GLB totally dissipates.

3.1.2 Layout and verification

While designing a standard cell it is very important to check if they are violating the rule sets that are to be followed for every cell that is being designed. The rules for checking are predefined in the EDA tool that we use. The DRC, the Design Rule Check is first performed to check if all the metal and other materials like poly and via are made with the specifications limit within which they are to be made. This rules if violated the design isn't valid and cannot be further used. The DRC check for NAND_GLB has been done and verified that the variation in the gate length has not brought about any variation in the range of values with which the cell is supposed to be manufactured. The foundry values are varied in such a way that it doesn't affect the device characteristics. The DRC for the design passed with no errors. After performing the DRC verification our design has to pass the Layout Versus Schematic check. This LVS check is run to verify if the layout mask that has been manually created by us matches the basic skeleton that we had expected. Our expected design is our golden design which was drawn using Virtuoso schematic editor. The virtuoso layout editor is used to draw the mask for the modified design. The functionality of both would be same only if it passes the LVS check.

3.1.3 Abstract view and LEF generation

Abstract view provides the details for placement and routing of the cell. The abstract view has the metal and pin information on it. The abstract view generation is done because the place and route tool does not require the full layout cell information. This view provides details about cell name, site name, orientation, PR boundary, Pin names, locations, pin metal layer, type and direction (input/output/input-output). Also provides location of all metal track and vias in the layout (obstructions). This information is passed to the P & R tool in the LEF format (Library Exchange Format). The LEF file contains technology information along with all the cell descriptions. We will use Cadence Abstract Generator tool for producing the abstract view from your standard cell layout view. Generating the abstract view has several steps like pin, extract, abstract and verify. They individually find several required information. The pin step extracts the pin information using the overlap text and metal technique. The extract step takes the path of all nets to one pin. The abstract step finds the obstacles on the path. Verify step is used to verify if the PR boundary has been created properly.

3.1.4 Standard cell characterization

A cell that is being created need to be verified for various factors. Normal verification of functionality takes

too long for which the method of characterization is done. The extraction of functionality is very complicated. Functional or delay simulation takes way too long. Power extraction also takes a long time. Automatic detection of timing constraints is also difficult. In order to avoid all these complexities we characterize our cell. This characterization process gives a simple model for delay, function, and power analysis.

3.1.5 Power, timing & area analysis

Power is the main motive of this work. The power that has been reduced when compared to the conventional NAND cell is being checked using power analysis. The power timing and area analysis was done using RC complier. The analysis thus proves that the power of the standard cell is less compared to the conventional one. The leakage power is reduced to an extend that when they are used in any digital logic circuit the total power dissipation caused due to leakage power is reduced. The analysis reports are placed for validation at the bottom of the discussion. The area has been increased to a few nm which would not bring about any drastic difference in the digital system. The timing also has increased by a very few ns which might be critical based on the applications that we use. Power in this case was also checked manually by obtaining the current and the voltage that the circuit uses.

Static Power

$$P=Vdd*Istat \quad (1)$$

Here the input of the circuit is 0 which explains how much power will be lost in a block when it is in its dormant mode. This finds the leakage due to sub threshold.

Total power is also calculated by taking the value of Vt and It from the calculator.

$$P=Vt*It. \quad (2)$$

3.1.6 Digital circuit implementation

The standard cell that has been designed with gate length varied is implemented in a 8 bit Multiplier Accumulator unit. This evidently verifies that the modified cell has high amount of improvement in power than the normal one. The MAC unit consists of three different blocks [2] the multiplier which is an array multiplier here, and an adder which is a normal adder and an accumulator which is a parallel in parallel out. The MAC unit implementation and its design are shown in the further parts of the discussion. Each unit has its own design being implemented with NAND gates. The critical paths are being identified and the rest are substituted with the modified standard cell. Here the work shows the comparison with itself. Both the modified and unmodified 8-bit MAC units were created to check the power variation and other factors too. The figure shows the MAC_GLB unit.

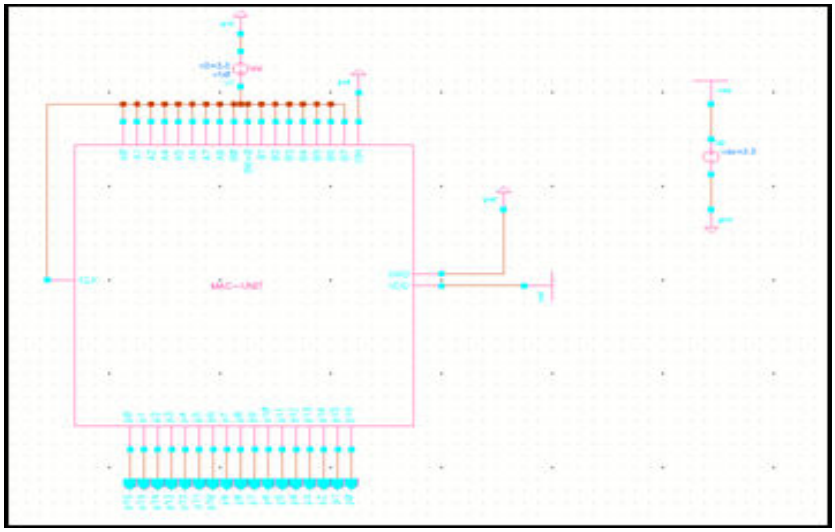

Figure-2. MAC_GLB unit.

In this digital implementation the newly designed standard cell NAND_GLB has been used in implementing the different blocks of the MAC unit. The power dissipated by the unmodified MAC is found to be more compared to the NAND_GLB based MAC unit. The MAC unit has different units like the 8 bit multiplier, 17 bit adder and 17 bit accumulator. Here for addition a normal adder is being used, for multiplier array multiplier is being used and as accumulator PIPO is being used. The leakage that occurs in all the block in both modified and unmodified are verified to conclude that our GLB technique is much more efficient.

4. RESULT ANALYSIS

The analysis part has two validations to be done one is to see how much power reduction does an individual NAND gate provide when the GLB technique is being used and the other one is to identify the power reduction in the MAC unit when the NAND_GLB cell is being used.

4.1 Comparison of NAND_GLB with conventional NAND gate

Table-1. NAND_GLB & NAND_Unmod comparison.

Factors	Leakage power (nW)	Total power (nW)	Delay (nS)	Area (nm)
NAND_Unmd	0.258	642.982	7.954	10
NAND_GLB	0.228	542.902	7.962	13
% Change	13.15	18.43	1	3

The table clearly shows the decrease in leakage power in one individual NAND cell. This NAND_GLB is then tried to implement at the application level. Here to verify it a 8 bit MAC unit is being used. The array multiplier of the MAC unit makes use of AND gates which are designed using the NAND_GLB and the adders are also designed using the modified NAND. They are placed on the non-critical paths. Similarly the adder and the accumulator are also created.

Table-2. MAC_GLB &MAC_Unmod comparison.

Factors	Leakage power(W)	Total power(mW)	Delay (nS)
MAC_Unmod	0.0304	16.381	0.153
MAC_GLB	0.0220	12.045	0.165
%Change	38	36	8

The comparisons of all individual units are represented in the form of a column chart which clearly analyses the improvement achieved.

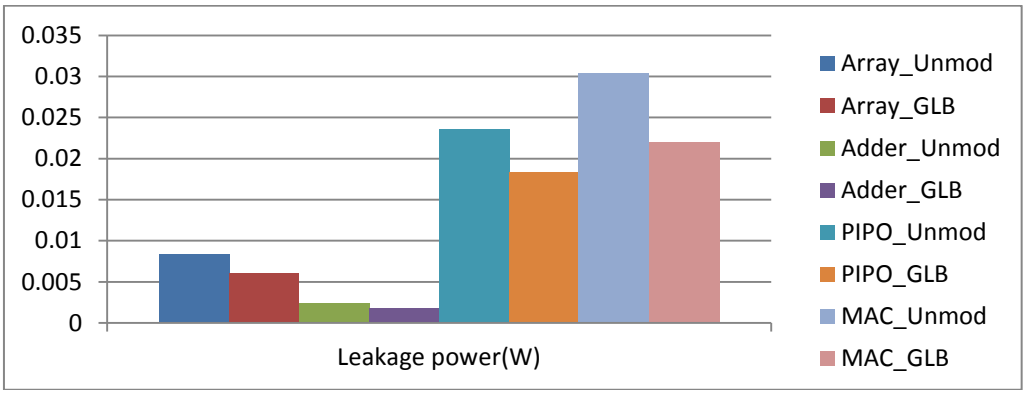

Figure-3. The column chat indicates the leakage power in all the units being used.

The column chart clearly shows the decrease in leakage power in every block when GLB technique is used.

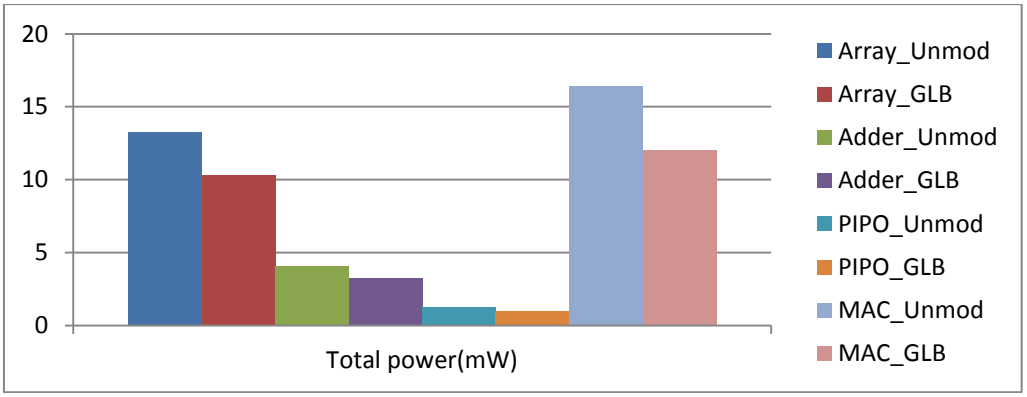

Figure-4. Depicts the total power comparison of each module and the MAC.

The MAC and each and every sub block have its power being depicted in the graph above. Every GLB module is found to have lesser power that the unmodified ones.

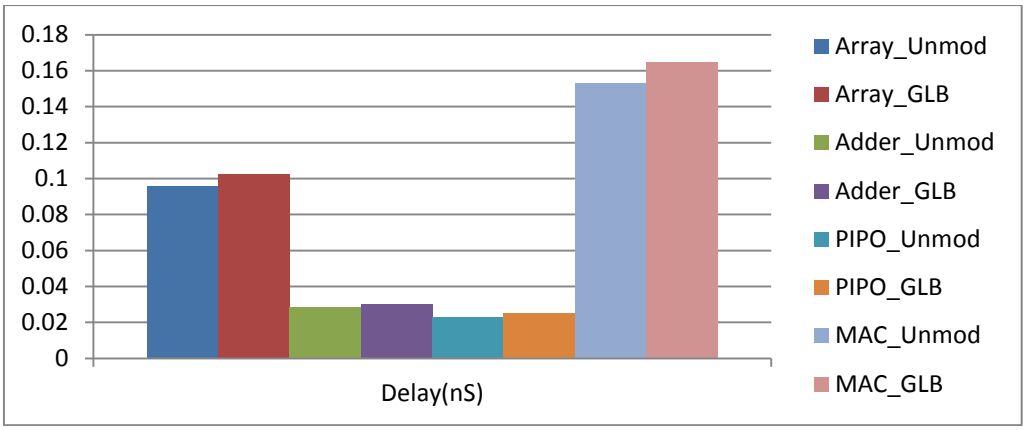

Figure-5. The delay penalty is depicted.

The delay comparison is shown in the figure which depicts that there is only a very little delay variation.

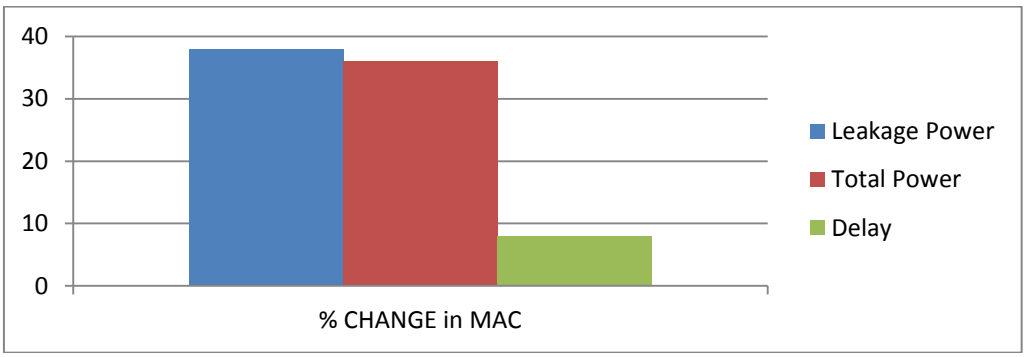

Figure-6. % Increase in MAC unit.

Thus this NAND_GLB is a standard cell that can be used for any other application for places where power reduction plays a major role.

5. CONCLUSIONS

After going through a continuous phase of struggle this project has come to a conclusion. The work has been validated and its objective has been proved. This project which aims in reducing the leakage power in any digital design and the same has been achieved and verified using a MAC unit.

Thus, we have studied about different forms to reduce power and why our design seems to be efficient compared to all the others. It's proved by this work that GLB technique has good power reduction with only a little penalty in area and delay. The proposed system which makes use of the GLB technique to build a standard cell like the NAND_GLB. Each NAND_GLB cell has 18.43% of power reduction and a leakage power reduction of 13.15%. The delay has just increased by 1%. Area has an increase of 3nm.

This power efficient NAND cell is used in a MAC unit and it is found that the total power is decreased by 36% and then leakage power is reduced by 38% with an increase in delay by 8%. The MAC with GLB technique has better power efficiency than the conventional MAC.

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